What is claimed is:

1. A self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

a non-inverting buffer chip for connection to one of said bit lines;

a resistor having a predetermined electrical resistance connected across said buffer chip; and

said chip and resistor having upper and lower voltage thresholds that cause said chip to change states when a level of voltage applied to said chip and said resistor passes through said thresholds.

2. A programmable system comprising:

a Digital Signal Processor for transceiving discrete electrical inputs;

a tri state data bus electrically connecting said Digital Signal Processor to a CPU;

said Digital Signal Processor and said CPU having difference rates at which they operate in performing their respective functions, and

self-locking data bus circuits connected to respective bit lines of said data bus for matching different operating rates of said Digital Signal Processor and said CPU.

3. The programmable system, according to claim 2, wherein said system further includes:

a Complex programmable logic device for transceiving discrete electrical signals;

tri state data buses electrically connecting said Complex Programmable Logic Device to said CPU and said Digital Signal Processor, said Complex Programmable Logic Device and said Digital Signal Processor having rates at which they operate in performing their respective functions that are different from that of said CPU; and

self-locking data bus circuits connected to respective bit lines of said tri state data buses for matching different operating rates of said Complex Programmable Logic Device and said Digital Signal Processor with that of said CPU.